Improvement of Power System Transient Stability using TCSC, SSSC and UPFC

Lokesh Garg[1] S.K. Agarwal[2] Vivek Kumar[3]

Abstract—This paper presents the transient stability enhancement of a multimachine system using series FACTS controllers. Series FACTS controller devices i.e. TCSC, SSSC and UPFC have been used in this paper for enhancing the transient stability of the system. Time domain simulations are carried on PSAT (Power System Analysis Tool box). The simulation results demonstrate that transient stability improves commendably of the multimachine system by using TCSC, SSSC and UPFC. Eigen values analysis also has been done during prefault condition, fault condition and with Series FACTS controllers i.e. TCSC, SSSC and UPFC. It also been observed that UPFC gives better transient stability enhancement as compared to TCSC and SSSC.

Keywords— Power System, PSAT, FACTS, UPFC, TCSC, SSSC, Transient Stability, IEEE 9 Bus, Multimachine System

1 *Introduction*

Power system stability control is an important aspect. In the event of large disturbances, sudden faults, opening or closing of circuit breaker, load changes etc or internal mechanical torques affects the power system stability of the system. Since power systems is a large interconnected system it is required that it must have secure and stable operation. In the last two decades the Flexible AC transmission system (FACTS) devices are becoming more popular. The main objectives of FACTS devices are to improve transient stability, voltage stability and line transfer capacity. Out of these three objectives the improvement of transient stability is one of the most important aspects [18}. Using FACTS devices the enhancement of transient stability can be done by controlling the real and reactive power during fault conditions. Blackout can occur if the system has low transient stability because of which the generators may go out of synchronism. Due to nonlinear characteristics of power system components, undesirable oscillations and transients are produced under small and large signal perturbations. In long transmission lines series compensation, shunt compensation, series and shunt compensation schemes are used in order to enhance the transient stability of the system as well as the power transfer capability .Due to advancement of solid state power electronic, FACTS devices have fast and reliable operation. Different types of FACTS devices are available like TCSC, SVC, SSSC, UPFC etc [5]. In this paper transient stability analysis has been done by using TCSC, SSSC and UPFC. The present paper is laid out as follows: Section I – Introduction, Section II- Study system, Section III- Simulation results using PSAT model on IEEE 9 bus system prefault condition, faulty condition and post fault condition with different types of FACTS Controllers.

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Simulations results show that the transient stability of the system can be enhanced by different types of series FACTS controllers. UPFC has better transient stability enhancement characteristics as compared to other series FACTS controllers' i.e TCSC and SSSC.

2 Study System

Prefault Condition

System under Study: In this model there are 9 Buses, Bus No. 1 is taken as Slack Bus, voltage at this bus is 1p.u. and buses 2 and 3 are Generator Buses (PV Buses). Generator 1 rated with 100MVA, 18KV and 60Hz, Generator 2 rated with 100MVA, 16.5KV and 60Hz, Generator 3 rated with100MVA, 13.8KV and 60Hz. Generator Data, Bus data, Line data has been given in the Appendix-I. IEEE 9 bus system used here as a multimachine system. Study system is shown in Figure No. 1 with prefault condition. All buses connected to each other by π section of transmission line. Assuming loads to be of constant impedance and all generators are operating with constant mechanical input power and with constant excitation. Power System Analysis Tool box (PSAT) software is used for the simulation. Transient stability is more in steady state condition i.e. prefault condition. The IEEE 9 bus system built using PSAT library. Rotor angle curve, Voltage at all buses during prefault condition is shown in figure 6 (a) and 6(f) respectively.

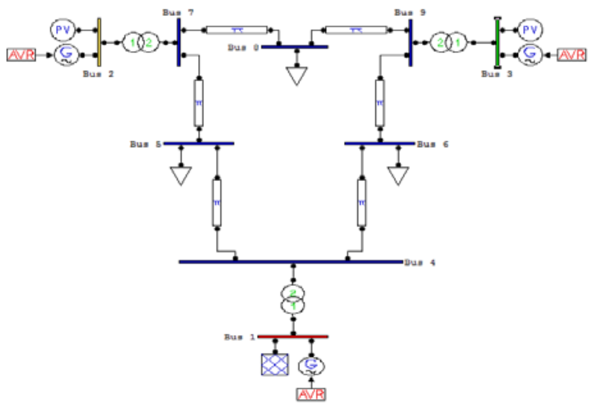

Figure: IEEE 9 Bus System Prefault Condition

Fault Condition

Athree phase fault is simulated at bus no. 4 after start of simulation 3s and the fault clearing time is 3.1s. As the fault occurs on the system there may be loss of synchronism between the generators. It also affects the voltage at all buses etc. during fault. Simulation result show that the rotor angle positions of different generators change with reference to prefault condition also the bus voltages at different buses has been changed with reference to prefault condition. Rotor angle curve, Voltage at all buses during fault condition is shown in figure 6 (b) and 6(g) respectively.

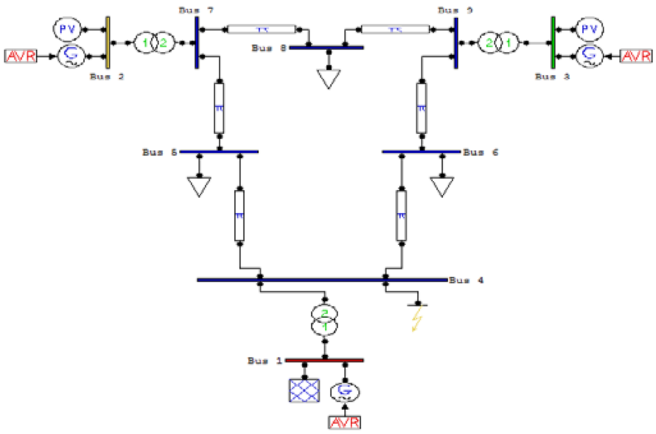

Figure2: IEEE 9 Bus System Fault Condition

Post Fault Condition with TCSC

In order to maintain the synchronism and also enhanced the transient stability of the system different types of series FACTS devices i.e TCSC, SSSC and UPFC are placed in the faulty system. TCSC has been place in between bus No. 4 and 5. TCSC having 30% series compensation has been used for simulation. TCSC data has been given in the Appendix-II. Rotor angle curve, Voltage at all buses in post fault condition is shown in figure 6 (c) and 6(h) respectively.

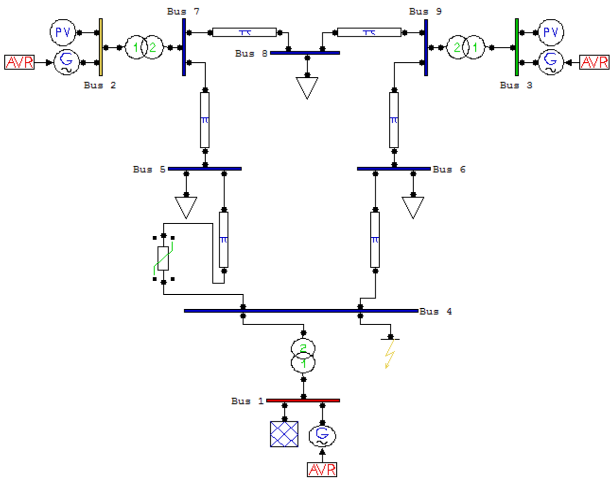

Fig.3 : IEEE 9 Bus System with TCSC

PostFault Condition with SSSC

In order to maintain the synchronism and enhanced transient stability of the system SSSC with 30% series compensation has been placed in the faulty system between bus no. 4 and 5. SSSC data has been given in the Appendix -II. Rotor angle curve, Voltage at all buses in post fault condition is shown in figure 6(d) and 6(i) respectively.

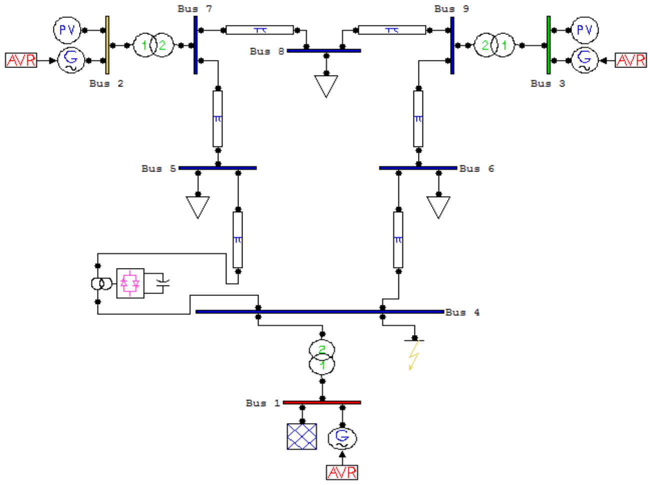

Figure4 : IEEE 9 Bus System with SSSC

PostFault Condition with UPFC

For enhancement of transient stability and to maintain the synchronism UPFC has been installed between bus no. 4 and 5 with 30% series compensation. UPFC data also has been given in the appendix.Rotor angle curve, Voltage at all buses in post fault condition is shown in figure 6(e) and 6(j) respectively.

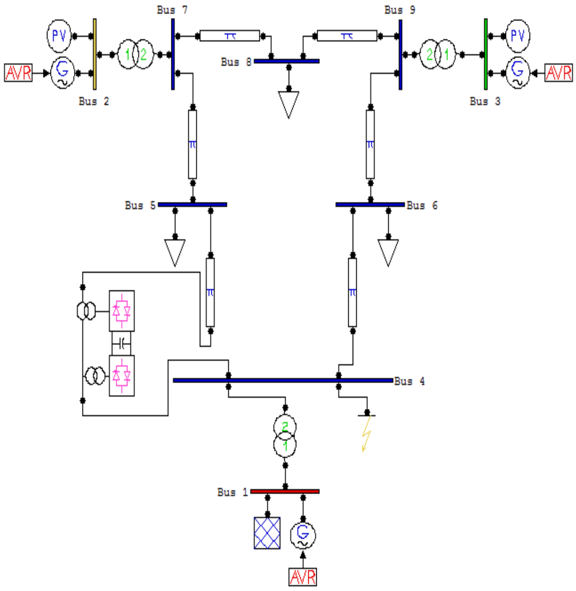

Figure 5 : IEEE 9 Bus System with UPFC

I- Simulation Results

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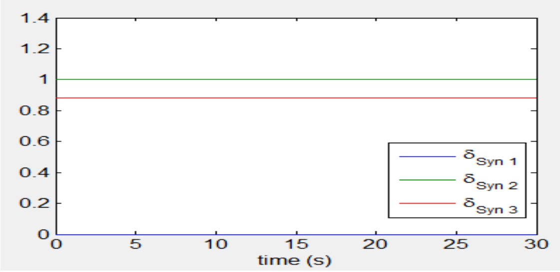

Fig.6 (a) : Rotor Angle Curve Prefault Condition

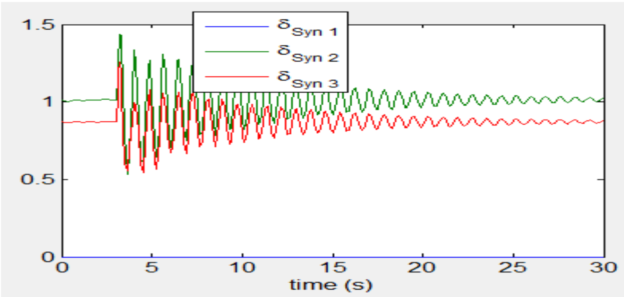

Fig. 6 (b) : Rotor Angle Curve fault Condition

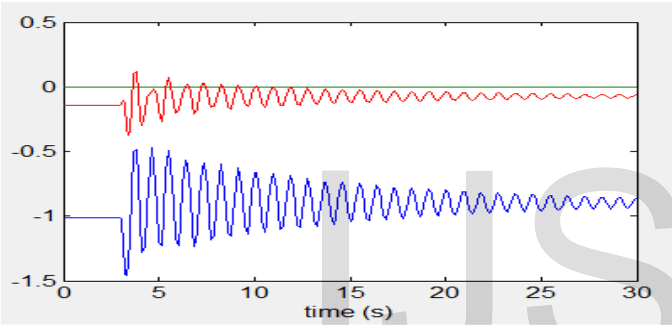

Fig. 6 (c) : Rotor Angle Curve with TCSC

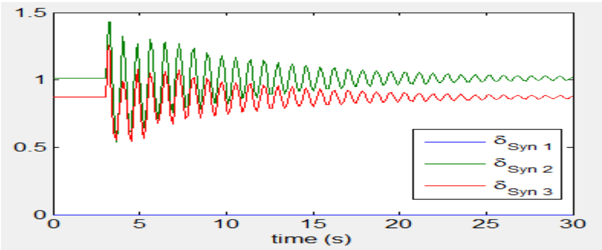

Fig. 6 (d) : Rotor Angle Curve with SSSC

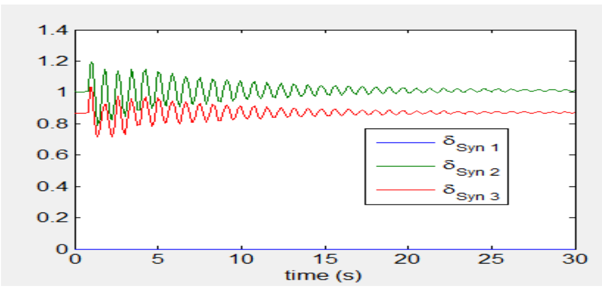

Fig. 6 (e) : Rotor Angle Curve with UPFC

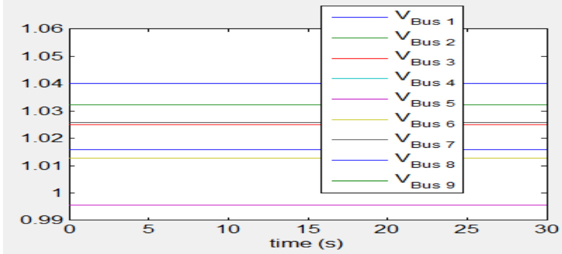

Fig.6 (f) : Voltage at all buses Prefault Condition

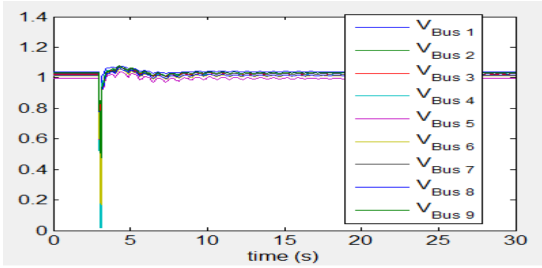

Fig. 16 (g) : Voltages at all Buses Fault Condition

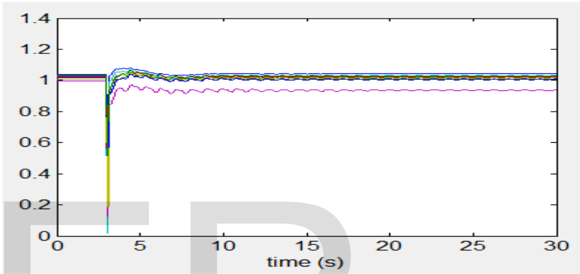

Fig.6 (h) : Voltage at all buses with TCSC

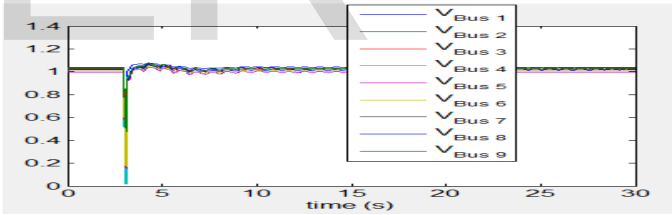

Fig.6 (i) : Voltage at all buses with SSSC

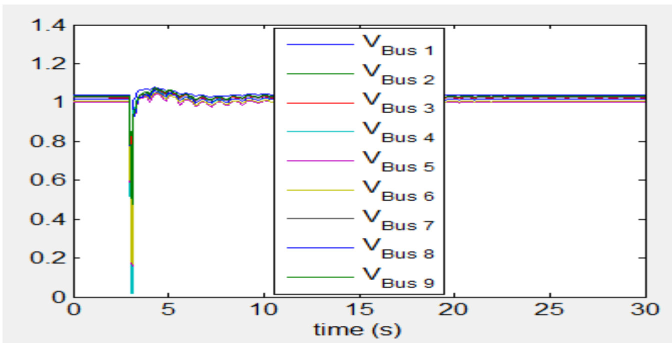

Fig.6 (j): Voltage at all buses with UPFC

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From simulation results from Fig 6 (a) to Fig 6 (j) shows the rotor angle curve, voltage at all buses with prefault condition, fault condition and post fault condition with different types of FACTS controllers'i.e TCSC, SSSC and UPFC.

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Appendix-I

GENERATOR DATA			
	GEN 1	GEN 2	GEN 3
MVA	100	100	100
KV	18	16.5	13.8
HZ	60	60	60
Ra (p.u.)	0.00	0.00	0.00
X_L (p.u.)	0.00	0.00	0.00
X_d (p.u.)	0.8958	0.1460	1.3125
X_d' (p.u.)	0.1198	0.0608	0.1813
X_d'' (p.u.)	0.0000	0.0000	0.0000
T'_{d0} (s)	6.00	8.96	5.89
T''_{d0} (s)	0.00	0.00	0.00
X_q (p.u.)	0.8645	0.0969	1.2578
X_q' (p.u.)	0.1969	0.0969	0.2500
X_q'' (p.u.)	0.0000	0.0000	0.0000
T'_{q0} (s)	0.5350	0.3100	0.6000
T''_{q0} (s)	0.0000	0.0000	0.0000

BUS DATA					
BUS NO.	NO. OF I/P	NO. OF O/P	Voltage (KV)	Voltage (p.u)	Angle (rad)
1	2	1	16.5	1.0	0.0
2	2	1	18	1.0	0.0
3	2	1	13.8	1.0	0.0
4	2	1	230	1.0	0.0
5	1	2	230	1.0	0.0
6	1	2	230	1.0	0.0
7	1	2	230	1.0	0.0
8	2	1	230	1.0	0.0
9	1	2	230	1.0	0.0

TRANSFORMER DATA ALL TRANSFORMERS 100MVA, 60HZ					
S. No.	FROM BUS	TO BUS	Impedance (p.u)		Pri./Sec. Voltage (KV)
			R(p.u.)	X(p.u.)	
1	1	4	0.00	0.0576	16.5/230
2	3	9	0.00	0.0586	13.8/230
3	2	7	0.00	0.0625	18/230

LINE DATA						
LINE No.	From Bus	To Bus	**Line impedance (p.u)**		Half line charging Susceptance B/2(p.u.)	MVA
			R (p.u.)	**X(p.u.)**		
1	4	5	0.01	0.085	0.0880	100
2	4	6	0.017	0.092	0.0790	100
3	5	7	0.032	0.161	0.1530	100
4	7	8	0.0085	0.072	0.7450	100
5	8	9	0.0119	0.1008	0.1045	100
6	6	9	0.039	0.170	0.1790	100

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EIGEN VALUE ANALYSIS					
	PRE FAULT	WITH FAULT	WITH TCSC	WITH SSSC	WITH UPFC
Dynamic Order	24	24	26	25	27
Buses	9	9	9	9	9
Positive Eigens	0	1	0	0	0
Negative Eigens	22	22	23	23	25
Complex Pairs	8	8	8	8	8
Zero Eigens	2	2	3	2	2

Appendix-II

FACTS CONTROLLER DATA			
	TCSC	**SSSC**	**UPFC**
MVA	100	100	100
KV	230	230	230
HZ	60	60	60
Operating Mode	Constant Power	Constant Reactance	Constant Reactance
% Series Compensation	30	30	30
Gain Kr (p.u.)	----	----	1.0
Time Constant (s)	0.5	12	0.1
V_pMax	----	0.1	0.05
V_pMin	----	0.02	0.01
V_qMax	----	----	0.02
V_qMin	----	----	0.01
I_qMax	----	----	0.1
I_qMax	----	----	0.02
Xc (max.)	0.5	----	----
Xc (min.)	-0.5	----	----
Kp	5	----	----
Ki	1	----	----
Gain for stabilising Signal (Kr)	10	----	----

EIGEN VALUE ANALYSIS					
S. No.	Prefault Condition	Fault Condition	With TCSC	With SSSC	With UPFC
1	-1000+J0	-1000+J0	-1000+J0	-1000+J0	-1000+J0
2	-1000+J0	-1000+J0	-1000+J0	-1000+J0	-1000+J0
3	-1000+J0	-1000+J0	-1000+J0	-1000+J0	-1000+J0
4	-0.720 + 12.745	-0.700 +j12.763	-0.740+ j1.267	-0.715 + j2.750	-0.711 + j12.758
5	-0.720- j12.745	-0.700 - j12.763	-0.740- j1.267	-0.715 - j2.750	-0.711 - j12.758
6	-0.190 + j8.365	-0.1534 +j8.290	-0.109 +j7.391	-0.1625 +j8.384	-0.1624 +j8.39
7	-0.190 - j 8.365	-0.1534 -j8.290	-0.109 -j7.391	-0.1625 -j8.384	-0.1624 -j8.39
8	-5.487 + j7.947	-5.4897 + j7.95	-5.552 + j7.982	-5.498 + j7.95	-5.4943 + j7.951
9	-5.487 - j7.947	-5.4897 - j7.95	-5.552 - j7.982	-5.498 - j7.95	-5.4943 - j7.951
10	-5.222 +j7.813	-5.2315 +j7.842	-5.225 +j7.844	-5.236+j7.844	-5.2366 +j7.847
11	-5.222 -j7.813	-5.2315 -j7.842	-5.225 -j7.844	-5.236 -j7.844	-5.2366 -j7.847
12	-5.323 + j7.920	-5.330 + j7.927	-5.339 + j7.923	-5.33 + j7.927	-5.3345 + j7.927
13	-5.323 - j7.920	-5.330 - j7.927	-5.339 - j7.923	-5.33 - j7.927	-5.3345 - j7.927
14	-5.178+j0	-5.1804 +j0	-5.006 +j0	-5.162 +j0	-5.1737 +j0
15	-3.3996+j0	-3.558 +j0	-3.431 +j0	-3.5762+j0	-3.5744 +j0
16	-0.443 + j1.211	-0.475 +j1.083	-0.485 +j1.079	-.4767+j1.078	-0.4760 +j1.078
17	-0.443 - j1.211	-0.475 -j1.083	-0.485 -j1.079	-0.476 -j1.078	-0.4760 -j1.078
18	-0.439 +j0.7394	-0.445 +j0.732	-0.462 +j0.814	-0.445+j0.7262	-0.4445+j0.7264
19	-0.439 -j0.7394	-0.445 -j0.732	-0.462 -j0.814	-0.445-j0.7262	-0.4445-j0.7264
20	-0.425 +j0.496	-0.425 +j0.493	-0.442+j0.515	-0.429 +j0.498	-0.4283 +j0.497
21	-0.425 -j0.496	-0.425 -j0.493	-0.4428 -j0.515	-0.429 -j0.498	-0.4283 -j0.497
22	0 + j0	0 + j0	0 + j0	0 + j0	0 + j0
23	0 + j0	0 + j0	0 + j0	0 + j0	-10 + j0
24	-3.225 +j 0	-3.225 +j 0	-3.2258 +j 0	-3.2258 +j 0	-3.2258 +j 0
25	----------------	----------------	-2 +j 0	----------------	-10 + j0
26	----------------	----------------	0 + j0	----------------	-10 + j0
27	----------------	----------------	----------------	----------------	-10 + j0